(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 975 011 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
26.01.2000 Bulletin 2000/04

(51) Int Cl.7: **H01L 21/20**, H01L 21/762

(21) Application number: **99305804.9**

(22) Date of filing: **22.07.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **23.07.1998 JP 20803398**
23.07.1998 JP 20803498
23.07.1998 JP 20803598

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(54) Semiconductor substrate and method of producing same

(57) In order to provide a semiconductor substrate that can be an SOI substrate suitable for production of high-frequency transistor, the semiconductor substrate is produced by a method of producing the semiconductor substrate having a step of bonding a first base having a semiconductor layer region to a second base and a step of removing the first base while leaving the semiconductor layer region on the second base, wherein a magnitude relation between the concentration of a p-type impurity and the concentration of an n-type impurity in the bonding atmosphere is established according to the composition of the second base.

FIG. 1A

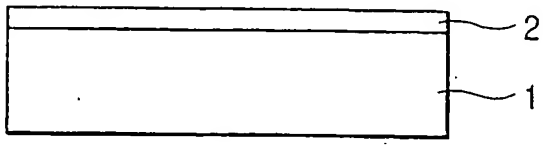

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FIG. 1B

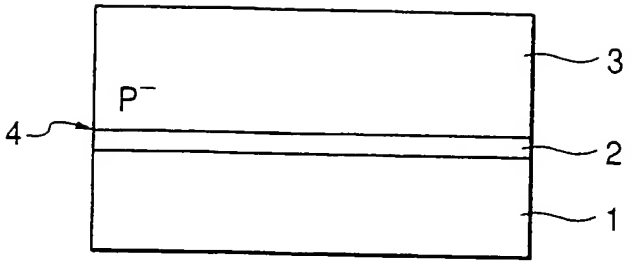
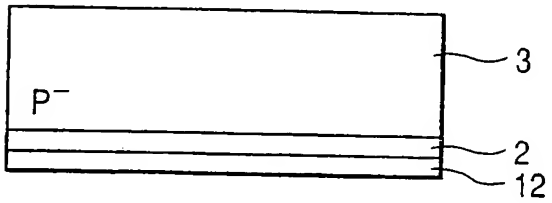


FIG. 1C



Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor substrate called an SOI substrate or the like and a method of producing the same.

Related Background Art

[0002] There are known methods for producing the SOI substrate having a single-crystal semiconductor thin film in such a manner that an Si wafer as a first base is bonded to another Si wafer as a second base with an insulating layer being interposed therebetween and a part of the first base on the back surface side is removed to make the single-crystal semiconductor thin film transferred onto the second base.

[0003] Particularly, the methods utilizing a porous layer, described in Japanese Patent Publication No. 2608351 and U.S. Pat. No. 5,371,037, are excellent methods to obtain an SOI substrate with good quality.

[0004] Further, U.S. Pat. No. 5,374,564 also describes a method of producing an SOI substrate making use of a layer with microbubbles (porous layer) formed by execution of ion implantation of hydrogen ions and a heat treatment.

[0005] The inventor prepared SOI substrates according to the description of the above patents. The inventor then made an MOS transistor using these SOI substrates and found that in application of this transistor to a high-frequency circuit, more improvement was required in high-frequency characteristics of the transistor and the circuit.

SUMMARY OF THE INVENTION

[0006] An object of the present invention is to provide a semiconductor substrate that can be an SOI substrate suitable for production of a high-frequency transistor, at a high yield.

[0007] Another object of the present invention is to provide a semiconductor substrate having a semiconductor layer region comprising a single-crystal semiconductor through an insulating layer on a support substrate comprising a semiconductor,

wherein the support substrate has such a composition that a semiconductor surface portion immediately below the insulating layer is a semiconductor having a resistivity of not less than 100 Ωcm and/or such a composition that the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof, and to provide a production method thereof.

[0008] Still another object of the present invention is to provide a method of producing a semiconductor substrate comprising a step of bonding a first base comprising a semiconductor layer region to a second base and a step of removing the first base while leaving the semiconductor layer region on the second base,

wherein according to the composition of the second base, a magnitude relation is established between the concentration of an n-type impurity and the concentration of a p-type impurity in an atmosphere for carrying out the bonding step.

[0009] Another object of the present invention is to provide a semiconductor device formed in a semiconductor substrate having a semiconductor layer region comprising a single-crystal semiconductor through an insulating layer on a support substrate comprising a semiconductor,

wherein the support substrate has such a composition that a semiconductor surface portion immediately below the insulating layer is a semiconductor having a resistivity of not less than 100 Ωcm and/or such a composition that the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof.

[0010] A method of producing a semiconductor substrate according to a preferred embodiment of the present invention is a method of producing a semiconductor substrate comprising a step of bonding a first base comprising a semiconductor layer region to a second base and a step of removing the first base while leaving the semiconductor layer region on the second base,

wherein the bonding step is carried out in an atmosphere in which the concentration of an n-type impurity is lower than the concentration of a p-type impurity, and wherein the second base is a base comprising a portion comprising an n-type semiconductor having a resistivity of not less than 100 Ωcm on the bonding surface side.

[0011] A method of producing a semiconductor substrate according to another preferred embodiment of the present invention is a method of producing a semiconductor substrate comprising a step of bonding a first base comprising a semiconductor layer region to a second base and a step of removing the first base while leaving the semiconductor layer region on the second base,

wherein the bonding step is carried out in an atmosphere in which the concentration of a p-type impurity is lower than the concentration of an n-type impurity, and wherein the second base is a base comprising a portion comprising a p-type semiconductor having a resistivity of not less than 100 Ωcm on the bonding surface side.

[0012] A method of producing a semiconductor substrate according to still another preferred embodiment of the present invention is a method of producing a semiconductor substrate comprising a step of bonding a first base comprising a semiconductor layer region to a second base and a step of removing the first base while

leaving the semiconductor layer region on the second base,

wherein the bonding step is carried out in an atmosphere in which the concentration of a p-type impurity is lower than the concentration of an n-type impurity, and wherein the second base is a base comprising a portion comprising an n-type semiconductor having a resistivity of not less than 300 Ωcm and having an insulating layer formed on the bonding surface side.

[0013] A semiconductor substrate according to a preferred embodiment of the present invention is a semiconductor substrate having a semiconductor layer region comprising a single-crystal semiconductor through an insulating layer on a support substrate comprising a semiconductor,

wherein the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof near the insulating layer.

[0014] Another semiconductor substrate according to a preferred embodiment of the present invention is a semiconductor substrate having a semiconductor layer region comprising a single-crystal semiconductor through an insulating layer on a support substrate comprising an n-type semiconductor,

wherein the support substrate has a region with decreasing resistivity toward the insulating layer in the direction of thickness thereof and wherein the resistivity of a portion immediately below the insulating layer is not less than 100 Ω·cm.

[0015] According to the present invention described above, the decrease of resistivity is restrained near the surface of the support substrate immediately below the insulating layer in the production of the SOI substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016]

Figs. 1A, 1B and 1C are schematic sectional views showing the steps of Embodiment 1 of the present invention;

Fig. 2 is a schematic, sectional view showing a bonding space provided in a clean room, as used in the present invention;

Fig. 3 is a graph showing the dependence of resistivity on the depth of various support substrates;

Figs. 4A, 4B, 4C and 4D are schematic sectional views showing the steps of Embodiment 2 of the present invention;

Figs. 5A, 5B, 5C and 5D are schematic sectional views showing the steps of Embodiment 3 of the present invention;

Figs. 6A, 6B and 6C are schematic sectional views showing the steps of Embodiment 4 of the present invention;

Fig. 7 is a schematic, sectional view showing a bonding space provided in a clean room, as used in the present invention;

Fig. 8 is a graph showing the dependence of resistivity on the depth of various support substrates;

Figs. 9A, 9B, 9C and 9D are schematic sectional views showing the steps of Embodiment 5 of the present invention;

Figs. 10A, 10B, 10C and 10D are schematic sectional views showing the steps of Embodiment 6 of the present invention;

Figs. 11A, 11B, 11C and 11D are schematic sectional views showing the steps of Embodiment 7 of the present invention;

Fig. 12 is a graph showing the dependence of resistivity on the depth of a support substrate in accordance with Embodiment 7 of the present invention;

Figs. 13A, 13B, 13C and 13D are schematic sectional views showing the steps of Embodiment 8 of the present invention;

Figs. 14A, 14B, 14C and 14D are schematic sectional views showing the steps of Embodiment 9 of the present invention;

Fig. 15 is a schematic sectional view showing a semiconductor substrate in accordance with the present invention;

Fig. 16 is a schematic sectional view showing a semiconductor device in accordance with the present invention;

Fig. 17 is a graph showing the dependence of resistivity on the depth of an SOI substrate in accordance with Example 1 of the present invention;

Fig. 18 is a graph showing the dependence of resistivity on the depth of an SOI substrate in accordance with Example 4 of the present invention; and

Figs. 19A, 19B, 19C and 19D are schematic sectional views showing the production steps of an SOI substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] In order to facilitate understanding of the present invention, the technological findings leading to the accomplishment of the present invention will be described prior to the description of the embodiments of the present invention.

(Experiment 1)

[0018] A first experiment of the method of producing the SOI substrate carried out by the inventor will be described by reference to Figs. 19A to 19D.

[0019] Prepared as a first base 1 is an Si wafer having a porous layer 11, a semiconductor layer region 12 made of a single-crystal semiconductor, and an insulating layer 2 made of silicon oxide (Fig. 19A).

[0020] Specifically, a surface of an Si wafer is changed into a porous surface by anodization, thereafter a semiconductor layer is epitaxially grown, and the

surface of the semiconductor layer region 12 undergoes thermal oxidation, thereby obtaining the Si wafer as illustrated in Fig. 19A.

[0021] Alternatively, the porous layer may also be made by thermally oxidizing the surface of the Si wafer and thereafter carrying out ion implantation of hydrogen ions to form microbubbles in the wafer.

[0022] Next, as illustrated in Fig. 19B, another Si wafer is prepared as a second base 10, for example, and a heat treatment is carried out at the temperature of about 900°C to 1200°C while a bonding surface of the insulating layer 2 of the above first base is kept in contact with a bonding surface of Si of the second Si wafer. This heat treatment effects bonding of the first and second bases 1, 10, thereby obtaining a multi-layer structure. Numeral 4 denotes a bonding interface.

[0023] Then, as illustrated in Fig. 19C, the porous layer 11 and the first base 1 on the back surface side thereof are removed by grinding, polishing, wet etching, or dry etching. Alternatively, the first base 1 is removed by splitting the bonded structure at the border of the porous layer 11.

[0024] The surface (exposed surface) of the semiconductor layer region 12 obtained in this way is a rough surface 19 due to the effect of the porous layer 11.

[0025] The rough surface 19 is smoothed by polishing or by a heat treatment in a reducing atmosphere containing hydrogen. Obtained in this way is the SOI substrate having the second base 10 of the Si wafer as a support substrate and the semiconductor layer region 12 of single-crystal Si thereon with the insulating layer (buried insulating layer) 2 therebetween.

[0026] More specifically, the first and second bases used in this Experiment 1 were CZ wafers of boron (B)-doped p-type single-crystal Si having the resistivity of 10 Ωcm, which were easiest to get. Then the SOI substrate was produced according to the steps described above.

[0027] The CZ wafers are wafers obtained from a single-crystal ingot formed by the Czochralski method.

[0028] Then a transistor circuit was fabricated using this SOI substrate.

[0029] However, this transistor circuit was inferior in high-frequency characteristics. The reason was that the resistance was low in the part being the support substrate (which was of the p-type CZ wafer) in the SOI substrate.

[0030] The high-frequency characteristics were degraded because of increase of parasitic capacitance in the structure of the SOI layer, the buried insulating film, and the support substrate of the SOI substrate, and increase of leak current.

[0031] If the support substrate is an insulator like silica glass the resistance of the support substrate can be kept high. Adoption of the insulator, however, does not present solution to all the issues.

[0032] Many systems for production of semiconductor devices arse produced for the purpose of processing bulk Si wafers such as the CZ wafers or the like. The silica glass is different from Si in such characteristics as thermal conductivity, coefficient of thermal expansion, light transmittance, and so on. Therefore, in the case of processing of the SOI substrate whose support substrate is made of the insulator like silica glass, process parameters of the apparatus for production of semiconductor devices have to be readjusted to a considerable degree. For the same reason, there are cases in which considerable change may be required for structure design and circuit design of semiconductor devices, and the like.

[0033] From these aspects, use of the semiconductor such as Si for the support substrate is more suitable for general purpose application.

(Experiment 2)

[0034] The SOI substrate was produced according to the aforementioned method, using wafers with a higher resistivity, for example, p-type FZ wafers having the resistivity of 1000 Ωcm, instead of the p-type CZ wafers. The transistor circuit was made using it, but the high-frequency characteristics expected were not achieved.

(Experiment 3)

[0035] Analysis was conducted as to impurity distribution of the SOI substrate produced in above Experiment 2. It was verified from the result that boron was detected in higher concentrations near the surface of the p-type FZ wafer immediately below the buried insulating layer and that the region of interest was thus of the p-type of a high impurity concentration and had the low resistance of about 1 Ωcm to 10 Ωcm.

(Experiment 4)

[0036] The concentration of boron and the concentration of phosphorus were measured in a space inside a clean room in which the bonding and heat treatment were carried out in Experiment 2.

[0037] The concentration of boron was 0.08 ng/liter, and the concentration of phosphorus less than 0.002 ng/liter.

[0038] Incidentally, the system was constructed in such structure that an HEPA (High Efficient Particulate Air) filter comprised of boron-containing glass fibers was used in the space inside the above clean room and clean air was supplied through the HEPA filter.

(Experiment 5)

[0039] The concentrations of boron and phosphorus were measured in a clean room in which clean air was supplied through a ULPA (Ultra Low Penetration Air) filter comprised of boron-free PTFE (polytetrafluoroethylene) and through a boron-adsorbing chemical filter.

[0040] The concentration of boron was less than 0.0003 ng/liter and the concentration of phosphorus less than 0.001 ng/liter.

[0041] The concentrations of arsenic and antimony were less than the detection limit and thus were negligible relative to the above boron concentration.

[0042] The HEPA filter, ULPA filter, and chemical filter are known, for example, in Japanese Patent Application Laid-Open Nos. 10-165730, 8-24551, and so on.

[0043] It became apparent from the results of the above experiments that to maintain the semiconductor surface part of the support substrate at a high resistance was able to be achieved at a high yield and readily by defining the magnitude relation between the concentration of a p-type impurity and the concentration of an n-type impurity in an atmosphere for execution of the bonding step, according to the composition of the base being the support substrate in the bonded semiconductor substrate.

[0044] Now production methods of semiconductor substrates will be described below according to three types of typical embodiments of the present invention.

[0045] Embodiments 1 to 3 are examples where the base becoming the support substrate is a high-resistance semiconductor of the p-type and where an atmosphere selected is one in which the concentration of a p-type impurity is lower than the concentration of an n-type impurity.

(Embodiment 1)

[0046] Figs. 1A to 1C show a method of producing a semiconductor substrate according to the present invention.

[0047] As illustrated in Fig. 1A, for example, the Si wafer is prepared as the first base 1 and the insulating layer 2 is formed on the surface thereof.

[0048] Prepared as a separate base from the first base is the second base 3 of a high-resistance p-type semiconductor having the resistivity of not less than 100 Ωcm.

[0049] The first base 1 having the insulating layer 2, and the second base 3, prepared as described above, are bonded to each other in a bonding atmosphere 20N as illustrated in Fig. 2. Numeral 4 designates the bonding interface.

[0050] Fig. 2 shows a bonding space provided in a clean room 23, in which 21N is a low-boron-releasing filter, for example such as the PTFE filter or the like, and/or a boron-adsorbing chemical filter, 22 a bulkhead, 24 a floor, and 30 a bonding device. The atmosphere 20N in this space is cleaned to the high cleanliness of class 1 of Federal Standard 209D of U.S.A. or a higher cleanliness as occasion may demand.

[0051] From the multi-layer structure obtained by bonding of the first base 1 and the second base 3, the first base is removed except for the semiconductor layer region 12 near the side of the insulating layer 2 of the first base by at least one removing method selected from grinding, polishing, etching, and so on.

[0052] Further, the substrate obtained is subjected to a heat treatment in a reducing atmosphere containing hydrogen, if necessary, thereby obtaining the SOI substrate illustrated in Fig. 1C.

[0053] Fig. 3 shows depth dependence of resistivity in various support substrates.

[0054] This figure shows resistivity profiles (P11, P12, P13) of support substrates where bonding was carried out in various atmospheres, using the p-type Si wafer having the resistivity of 300 Ωcm as the second base, and a resistivity profile (C11) of a support substrate where an n-type Si wafer was used as the second base.

[0055] P11 indicates the resistivity profile where the concentration Cn of an n-type impurity moving (penetrating) from the bonding atmosphere into the second base is two times the concentration Cp of a p-type impurity contained in the second base, P12 the resistivity profile where Cn is equal to Cp, and P13 the resistivity profile where Cn is 0.1 times Cp.

[0056] P11 to P13 all show the profiles in which the resistivity becomes higher toward the surface of the support substrate, i.e., toward the interface with the insulating layer, and, therefore, they are left-increasing profiles in Fig. 3 in the vicinity of the buried insulating layer (at least within 2 μm from the interface).

[0057] Particularly, P13 has no region where the profile becomes decreasing to the left and has the higher resistivity near the interface than that of the bulk. Therefore, P13 is more preferable.

[0058] In the case where the n-type wafer having the resistivity of 300 Ωcm is used as the second base, as indicated by C11, the n-type impurity diffuses from the bonding atmosphere into the wafer to decrease the resistivity near the interface considerably.

[0059] The bonding atmosphere used in the present invention does not mean only the atmosphere at the place where the bonding is carried out actually, but also means an atmosphere to determine a deposition state of impurities on the actual bonding surface. Namely, where the concentration of a p-type or n-type impurity in the actual bonding atmosphere is so very low as not to cause decrease of resistivity, it is dependent on an atmosphere immediately before placement of the second base in that atmosphere. In that case, therefore, the atmosphere immediately before the placement can also be regarded as a bonding atmosphere.

[0060] The concentration (Nn) of an n-type impurity in the bonding atmosphere is preferably not more than 0.1 ng/liter and more preferably not more than 0.01 ng/liter and the concentration (Np) of a p-type impurity ip the bonding atmosphere is preferably not more than 0.01 ng/liter and more preferably not more than 0.001 ng/liter. In addition, it is necessary to satisfy the relation of Nn > Np.

[0061] As long as the relation of Nn > Np is met, lower limits of Nn, Np do not have to be defined; however, in

order to facilitate management of the atmosphere and restrain the production and running cost, Nn and Np both are preferably not less than 0.0001 ng/liter.

[0062] The above atmosphere can be an atmosphere formed in a clean room or in a local clean room of a high cleanliness placed in another clean room, or an atmosphere formed in a closed chamber.

[0063] In the former case, the principal component of the atmosphere is the clean air of the high cleanliness of class 1 level as mentioned above, and in the latter case, the principal component of the atmosphere can be an inert gas such as nitrogen, argon, helium, neon, or xenon, or oxygen.

[0064] For example, in the case of a clean room using the boron-releasing HEPA filter without use of the PTFE filter, B_2O_3 contained in the filter-constituting glass reacts with hydrofluoric acid (HF) in the clean room to evolve boron fluoride (BF_3) ($B_2O_3 + 6HF \rightarrow 2BF_3 + 3H_2O$).

[0065] In the bonding atmosphere of the clean room, the boron concentration is much greater than 0.01 ng/liter and is higher than the phosphorus concentration in the same atmosphere accordingly. Therefore, when the bonding is carried out in such an atmosphere, the resistivity profile will be one similar to that of C11 of Fig. 3 even if the high-resistance p-type wafer is used as the second base as in Experiments 2 and 3.

[0066] The second base used in the present invention is of a base material containing at least a region comprising a p-type semiconductor having a resistivity of not less than 100 Ωcm, more preferably not less than 500 Ωcm, and still more preferably not less than 1000 Ωcm on the bonding surface side.

[0067] Particularly, an Si wafer with the above resistivity produced by the floating zone process (FZ wafer) is preferably used as the second base, but the second base may be a CZ wafer.

[0068] Further, it is also preferable to form the insulating layer on the surface of the above second base and thereafter bond the first base thereto with the surface of the insulating layer as a bonding surface.

[0069] In this case, since this insulating layer acts as a barrier against penetration of a p-type impurity, the region immediately below the buried insulating layer becomes more resistant to decrease of the resistivity. Silicon oxide is preferably used as such an insulating layer, and the thickness of the insulating layer enough for the action as the barrier is not less than 100 nm and more preferably not less than 200 nm nor more than 10 μm.

[0070] The two bases can be bonded to each other more easily without formation of voids or the like at the bonding interface when one of the bonding surfaces of the first and second bases to be bonded is a surface of a semiconductor of Si or the like and the other is a surface of an insulator such as silicon oxide or the like.

[0071] In cases where two surfaces each comprised of an insulator are bonded to each other, it is desirable to bond them after an element such as oxygen, nitrogen, silicon, or the like is introduced into at least one of the bonding surfaces by plasma ion implantation or the like.

(Embodiment 2)

[0072] Next described is Embodiment 2 resulting from partial modification of Embodiment 1 described above. Reference is made to "J. Electrochem. Soc., Vol. 142, No. 9, September 1995, pp. 3116-3122" as to the details of the method of producing an SOI substrate using the porous layer.

[0073] A surface of a p-type Si wafer as the first base 1 is anodized to make the surface porous. Then a semiconductor layer region of non-porous single-crystal Si is formed on the porous surface by epitaxial growth.

[0074] Then the surface of the semiconductor layer region 12 is oxidized to form the insulating layer 2 as occasion may demand.

[0075] In this way, the first base is obtained as illustrated in Fig. 4A.

[0076] The second base 3 like the p-type FZ Si wafer with a high resistivity described in Embodiment 1 is prepared and is placed, together with the first base, in the bonding atmosphere where the p-type impurity concentration is low (Np < Nn). In the atmosphere they are placed so that the surface of the insulating layer 2 is in close contact with the surface of the p-type FZ Si wafer. At this time a heat treatment at 900°C to 1200°C is carried out as occasion may demand. In this way the multilayer structure as illustrated in Fig. 4B is obtained.

[0077] After that, the non-porous part on the surface side of the first base 1 is removed by grinding, polishing, or etching and the porous layer 11 is removed by selective wet etching with an etchant containing hydrogen fluoride and hydrogen peroxide, thereby obtaining the SOI substrate as illustrated in Fig. 4C.

[0078] Alternatively, a fluid or a wedge is driven against or into the side face of the multi-layer structure, or tension is applied in directions to separate the first base and the second base from each other, or the like, whereby the two members are separated from each other at the border of the porous layer with a low mechanical strength, thereby obtaining an SOI substrate with the semiconductor layer region 12 being left on the second base.

[0079] Further, the substrate is subjected to a heat treatment in a reducing atmosphere of hydrogen 100 % or in a reducing atmosphere of hydrogen diluted with an inert gas for one or more hours, whereby the rough surface 19 of the semiconductor layer region is smoothed so that the surface roughness of the SOI substrate becomes sufficiently smooth to Rrms not more than 5 nm.

[0080] The SOI substrate as illustrated in Fig. 4D is obtained in this way.

[0081] Since in this SOI substrate the support substrate 3 below the buried insulating layer 2 has a sufficiently high resistivity of not less than 100 Ω·cm, the transistor produced with this SOI substrate has less leak

current and can operate at a high speed.

(Embodiment 3)

[0082] Embodiment 3 is also an example resulting from partial modification of Embodiment 1.

[0083] As illustrated in Fig. 5A, the insulating layer 2 is formed on the surface of the first base 1 comprised of a semiconductor such as the Si wafer.

[0084] As illustrated in Fig. 5B, hydrogen ions or rare gas ions are implanted by ion implantation in the region about 100 nm to 2 μm below the lower surface of the insulating layer 2 of the first base 1 to form an ion-implanted layer 15 for creation of microbubbles. After that, it may be subjected to a heat treatment at 100°C to 400°C to evolve the microbubbles in the ion-implanted layer 15 if necessary.

[0085] As illustrated in Fig. 5C, the second base 3, which is comprised of a semiconductor like a high-resistance p-type Si wafer or the like as described in Embodiment 1, is prepared and is brought into close contact with the insulating layer 2 in the atmosphere 20N illustrated in Fig. 2. Then the substrate is subjected to a heat treatment at 500°C to 1200°C to aggregate the microbubbles evolved in the ion-implanted layer 15 or to newly evolve and aggregate the microparticles therein. Then the ion-implanted layer becomes fragile, and the first base 1 of the multi-layer structure is separated at the border of the ion-implanted layer 15 while the semiconductor layer region 12 is left.

[0086] Then the exposed surface of the semiconductor region 12 is smoothed by polishing or by a heat treatment in a reducing atmosphere containing hydrogen to obtain the SOI substrate with relatively good quality, though inferior to that of Embodiment 1, as illustrated in Fig. 5D.

[0087] The SOI substrate thus obtained is one with the support substrate having the resistivity profile as indicated by either of P11 to P13 of Fig. 3, depending on the penetration amount of impurities or the distribution state thereof.

[0088] Embodiments 4 to 6 described below are examples where an n-type high-resistance semiconductor is used as the support substrate and where the atmosphere selected is one in which the concentration of an n-type impurity is lower than the concentration of a p-type impurity.

(Embodiment 4)

[0089] Figs. 6A to 6C show another method of producing a semiconductor substrate according to the present invention.

[0090] As illustrated in Fig. 6A, for example, an Si wafer is prepared as the first base 1 and an insulating layer 2 is formed on the surface thereof.

[0091] Prepared as a separate base from the first base is the second base 13 of a high-resistance n-type semiconductor having the resistivity of not less than 100 Ωcm.

[0092] The first base 1 having the insulating layer 2, and the second base 13, prepared as described above, are bonded to each other in a bonding atmosphere 20P as illustrated in Fig. 7. Numeral 4 designates the bonding interface.

[0093] Fig. 7 shows the bonding space provided in clean room 23, in which 21P is a boron-releasing filter, for example such as the HEPA filter or the like, 22 the bulkhead, 24 the floor, and 30 the bonding device. The atmosphere 20P in this space is cleaned to the cleanliness of class 1 to 100 of Federal Standard 209D of U. S.A. as occasion may demand.

[0094] From the multi-layer structure obtained by bonding of the first base 1 and the second base 13, the first base is removed except for the semiconductor layer region 12 near the side of the insulating layer 2 of the first base by one of the removing methods as discussed in above Embodiment 1.

[0095] Further, the substrate obtained is subjected to a heat treatment in a reducing atmosphere containing hydrogen if necessary, thereby obtaining the SOI substrate illustrated in Fig. 6C.

[0096] Fig. 8 shows depth dependence of resistivity in various support substrates.

[0097] Fig. 8 shows resistivity profiles (P21, P22) of support substrates where the n-type Si wafer having the resistivity of 150 Ωcm was used as the second base, and a resistivity profile (C21) of a support substrate where the p-type Si wafer was used as the second base.

[0098] P21 indicates the resistivity profile where the concentration Cp of a p-type impurity to penetrate from the bonding atmosphere into the second base was equal to the concentration Cn of an n-type impurity contained in the second base, and P22 the resistivity profile where the insulating layer was formed on the surface of the second base before the bonding.

[0099] P21 and P22 all show the profiles in which the resistivity becomes higher toward the surface of the support substrate, i.e., toward the interface with the insulating layer, and, therefore, they are left-increasing profiles in Fig. 8 in the vicinity of the buried insulating layer (at least within 3 μm from the interface).

[0100] Particularly, P22 has no region where the profile becomes decreasing to the left and has the higher resistivity near the interface than that of the bulk. Therefore, P22 is more preferable.

[0101] In the case where the p-type wafer having the resistivity of 150 Ωcm is used as the second base as indicated by C21, the p-type impurity diffuses from the bonding atmosphere into the wafer to decrease the resistivity near the interface considerably.

[0102] The bonding atmosphere used in the present invention does not mean only the atmosphere at the place where the bonding is carried out actually, but also means an atmosphere to create the actual bonding surface. Namely, where the concentration of a p-type or n-

type impurity in the actual bonding atmosphere is so low as not to cause decrease of resistivity, it is dependent on an atmosphere immediately before placement of the second base in that atmosphere. In that case, therefore, the atmosphere immediately before the placement can also be regarded as a bonding atmosphere.

[0103] The concentration (Np) of a p-type impurity in the bonding atmosphere is preferably not more than 0.05 ng/liter and more preferably not more than 0.004 ng/liter and the concentration (Nn) of an n-type impurity in the bonding atmosphere is preferably not more than 0.01 ng/liter and more preferably not more than 0.002 ng/liter. In addition, it is necessary to satisfy the relation of $Nn < Np$.

[0104] As long as the relation of $Nn < Np$ is met, lower limits of Nn, Np do not have to be defined; however, in order to facilitate management of the atmosphere and restrain the production and running cost, Nn and Np both are preferably not less than 0.001 ng/liter, for which an expensive and high-performance filter does not have to be used.

[0105] The above atmosphere can be an atmosphere formed in a clean room or in a local clean room of a high cleanliness placed in another clean room, or an atmosphere formed in a closed chamber.

[0106] In the former case, the principal component of the atmosphere is the clean air of cleanliness of class 1 to 1000 level as mentioned above, and in the latter case, the principal component of the atmosphere can be an inert gas such as nitrogen, argon, helium, neon, or xenon, or oxygen.

[0107] For example, when the boron-releasing HEPA filter is used as in Experiment 4, the boron concentration in the bonding atmosphere 20P of Fig. 7 becomes higher than the phosphorus concentration in the same atmosphere 20P. Therefore, when the p-type high-resistance wafer is used as the second base in the bonding in this atmosphere as in Experiments 2, 3, the resistivity profile thereof is the result as indicated by C21 of Fig. 8.

[0108] The second base used in the present invention is a base material containing at least a region comprising an n-type semiconductor having the resistivity not less than 100 Ωcm, more preferably the resistivity of not less than 500 Ωcm, and still more preferably the resistivity of not less than 1000 Ωcm on the bonding surface side.

[0109] When the insulating layer as a barrier is not formed, there are cases in which it is preferable to use the n-type semiconductor having the resistivity not less than 100 Ωcm nor more than 500 Ωcm, as the second base. Particularly, the FZ wafer with the above resistivity is preferably used, but the CZ wafer can also be applicable.

[0110] Further, it is also preferable to form the insulating layer on the bonding surface side of the above second base and thereafter bond the first base thereto with the surface of the insulating layer as a bonding surface.

[0111] In this case, since this insulating layer acts as a barrier against penetration of a p-type impurity, the region immediately below the buried insulating layer becomes more resistant to decrease of the resistivity. Silicon oxide is preferably used as such an insulating layer, and the thickness of the insulating layer enough for the action as a barrier is not less than 100 nm and more preferably not less than 200 nm nor more than 10 μm.

[0112] The two bases can be bonded to each other more easily without formation of voids or the like at the bonding interface when one of the bonding surfaces of the first and second bases to be bonded is a surface comprised of a semiconductor of Si or the like and the other is a surface comprised of an insulator such as silicon oxide or the like.

[0113] In cases where surfaces of insulators are bonded to each other, it is desirable to bond them after an element such as oxygen, nitrogen, silicon, or the like is introduced into at least one of the bonding surfaces.

(Embodiment 5)

[0114] Next described is Embodiment 5 resulting from partial modification of Embodiment 4 described above.

[0115] The surface of the p-type Si wafer as the first base 1 is anodized to make the surface porous. Then the semiconductor layer region of non-porous single-crystal Si is formed on the porous surface by epitaxial growth.

[0116] Then the surface of the semiconductor layer region 12 is oxidized to form the insulating layer 2 as occasion may demand.

[0117] In this way, the first base is obtained as illustrated in Fig. 9A.

[0118] The second base 13 like the n-type FZ Si wafer with a high resistivity described in Embodiment 4 is prepared and is placed, together with the first base, in the bonding atmosphere where the n-type impurity concentration is low ($Np > Nn$). In the atmosphere they are placed so that the surface of the insulating layer 2 is in close contact with the surface of the n-type FZ wafer. At this time a heat treatment at 900°C to 1200°C is carried out as occasion may demand. In this way the multi-layer structure as illustrated in Fig. 9B is obtained.

[0119] After that, the non-porous part on the surface side of the first base 1 is removed by grinding, polishing, or etching and the porous layer 11 is removed by selective wet etching with an etchant containing hydrogen fluoride and hydrogen peroxide, thereby obtaining the SOI substrate as illustrated in Fig. 9C.

[0120] Alternatively, a fluid or a wedge is driven against or into the side face of the multi-layer structure, or tension is applied in directions to separate the first base and the second base from each other, or the like, whereby the two members are separated from each other at the border of the porous layer with low mechanical strength, thereby obtaining the SOI substrate with the semiconductor layer region 12 being left on the second base 13.

[0121] Further, the substrate is subjected to a heat treatment in a reducing atmosphere of hydrogen 100 % or in a reducing atmosphere of hydrogen diluted with an inert gas for one or more hours, whereby the rough surface of the semiconductor layer region is smoothed so that the surface roughness of the SOI substrate becomes sufficiently smooth to Rrms not more than 5 nm.

[0122] The SOI substrate as illustrated in Fig. 9D is obtained in this way.

[0123] Since in this SOI substrate the support substrate 13 below the buried insulating layer 2 has the sufficiently high resistivity of not less than 100 Ω·cm, the transistor produced with this SOI substrate has less leak current and can act at a high speed.

(Embodiment 6)

[0124] Embodiment 6 is also an example resulting from partial modification of Embodiment 4.

[0125] As illustrated in Fig. 10A, the insulating layer 2 is formed on the surface of the first base 1 comprised of a semiconductor such as the Si wafer.

[0126] As illustrated in Fig. 10B, hydrogen ions or rare gas ions are implanted by ion implantation in the region about 100 nm to 2 μm below the lower surface of the insulating layer 2 of the first base 1 to form an ion-implanted layer 15 for creation of microbubbles. Then, it may be subjected to a heat treatment at 100°C to 400°C to evolve the microbubbles in the ion-implanted layer 15 if necessary.

[0127] As illustrated in Fig. 10C, the second base 13, which is comprised of a semiconductor such as the high-resistance p-type Si wafer or the like as described in Embodiment 4, is prepared and is brought into close contact with the insulating layer 2 in the atmosphere 20P illustrated in Fig. 7. Then the substrate is subjected to a heat treatment at 500°C to 1200°C to aggregate the microbubbles evolved in the ion-implanted layer 15 or to newly evolve and aggregate the microparticles therein. Then the ion-implanted layer becomes fragile, and the first base 1 of the multi-layer structure is separated at the border of the ion-implanted layer 15 while the semiconductor layer region 12 is left.

[0128] Then the exposed surface of the semiconductor region 12 is smoothed by polishing or by a heat treatment in a reducing atmosphere containing hydrogen to obtain the SOI substrate with relatively good quality, though inferior to that of Embodiment 4, as illustrated in Fig. 10D.

[0129] The SOI substrate thus obtained is one with the support substrate having the resistivity profile as indicated by either P21 or P22 of Fig. 8, depending on the penetration amount of impurities or the distribution state thereof.

[0130] Embodiments 7 to 9 described below are examples where the base becoming the support substrate is a high-resistance n-type semiconductor with an insulating film and where the atmosphere selected is one in which the concentration of a p-type impurity is lower than the concentration of an n-type impurity.

(Embodiment 7)

[0131] Figs. 11A to 11D show another method of producing a semiconductor substrate according to the present invention.

[0132] As illustrated in Fig. 11A, the second substrate 16 prepared is one of a high-resistance n-type semiconductor having the resistivity of not less than 300 Ωcm, and the insulating layer 5 is formed at least on the upper surface thereof.

[0133] As illustrated in Fig. 11B, for example, the Si wafer is prepared as the first base 1.

[0134] The second base 16 having the insulating layer 5 on the bonding surface side, and the first base 1, prepared in this way, are bonded in the bonding atmosphere 20N as illustrated in Fig. 2. Numeral 4 designates the bonding interface.

[0135] Fig. 2 shows the bonding space provided in the clean room 23, in which 21N is the low-boron-releasing filter, for example such as the PTFE filter or the like, and/or the boron-adsorbing chemical filter, 22 the bulkhead, 24 the floor, and 30 the bonding device. The atmosphere 20N in this space is cleaned to the high cleanliness of class 1 as mentioned above or a higher cleanliness as occasion may demand.

[0136] From the multi-layer structure obtained by bonding of the first base 1 and the second base 16, the first base is removed except for the semiconductor layer region 12 near the side of the insulating layer 5 of the first base by one of the removing methods as in Embodiment 1.

[0137] Further, the substrate obtained is subjected to a heat treatment in a reducing atmosphere containing hydrogen if necessary, thereby obtaining the SOI substrate illustrated in Fig. 11D.

[0138] Fig. 12 shows depth dependence of resistivity in a support substrate according to the present embodiment.

[0139] Fig. 12 shows the resistivity profile (P31) of the support substrate where the bases were bonded to each other in an atmosphere containing a relatively large amount of an n-type impurity, using an n-type Si wafer of the resistivity 6000 Ωcm with the insulating layer formed on the surface, as the second base, and the resistivity profile (C31) of a support substrate as a comparative example.

[0140] P31 indicates the resistivity profile of the support substrate according to the present invention.

[0141] P31 demonstrates a profile in which the resistivity gradually decreases toward the interface with the insulating layer, i.e., a left-decreasing profile in Fig. 12, in the vicinity of the part immediately below the buried insulating layer (at least within 0.3 μm from the interface).

[0142] Particularly, in the case of P31, since the insu-

lating layer 5 is formed on the second base before the bonding, this insulating layer acts to impede penetration of an impurity, so that there is little decrease of the resistivity near the interface.

[0143] As indicated by C31, in cases where the n-type wafer having the resistivity of 6000 Ωcm is used as the second base and where the bases are bonded to each other without forming the insulating layer as a barrier on the bonding surface of the second base, because the second base itself is the semiconductor of the low impurity concentration, more n-type impurity diffuses from the bonding atmosphere into the n-type wafer to form a region of relatively strong n-type near the interface and decrease the resistivity considerably even if the adsorption amount of the n-type impurity is extremely small (~ 1×10^{11} atoms/cm^2).

[0144] The bonding atmosphere used in the present invention does not mean only the atmosphere at the place where the bonding is carried out actually, but also means an atmosphere to create the actual bonding surface. Namely, where the concentration of a p-type or n-type impurity in the actual bonding atmosphere is so low as not to cause decrease of resistivity, it is dependent on an atmosphere immediately before placement of the second base in that atmosphere. In that case, therefore, the atmosphere immediately before the placement can also be regarded as a bonding atmosphere.

[0145] The concentration (Nn) of an n-type impurity in the bonding atmosphere is preferably not more than 0.1 ng/liter and more preferably not more than 0.01 ng/liter and the concentration (Np) of a p-type impurity in the bonding atmosphere is preferably not more than 0.01 ng/liter and more preferably not more than 0.001 ng/liter. In addition, it is necessary to satisfy the relation of Nn > Np.

[0146] As long as the relation of Nn > Np is met, it is not significant to define the lower limits of Nn, Np; however, in order to facilitate management of the atmosphere and restrain the production and running cost, Nn and Np both are preferably not less than 0.0001 ng/liter, for example, by decreasing exchange frequency of filters.

[0147] The above atmosphere can be an atmosphere formed in a clean room or in a local clean room of a high cleanliness placed in another clean room, or an atmosphere formed in a closed chamber.

[0148] In the former case, the principal component of the atmosphere is the clean air of the high cleanliness of class 1 level as mentioned above, and in the latter case, the principal component of the atmosphere can be an inert gas such as nitrogen, argon, helium, neon, or xenon, or oxygen.

[0149] For example, in cases where the boron-releasing HEPA filter is used without using the PTFE filter, the boron concentration in the bonding atmosphere of the clean room becomes much higher than 0.01 ng/liter and higher than the phosphorus concentration in the same atmosphere. Therefore, when the bonding is carried out in such an atmosphere, it is hard to use the high-resistance p-type wafer as the second base. The reason is that the surface on the bonding surface side tends to become of much stronger p-type. In such cases the resistivity profile will have the surface side of lower resistance as indicated by C31 of Fig. 12.

[0150] The second base used in the present invention is a base having at least the bonding surface covered with an insulating layer and having at least a region comprising an n-type semiconductor immediately below the insulating layer, the n-type semiconductor having the resistivity of not less than 300 Ωcm, more preferably the resistivity of not less than 500 Ωcm, and still more preferably the resistivity of not less than 1000 Ωcm. Particularly, an FZ Si wafer with the above resistivity having the surface covered with the insulating layer is preferably used, but a CZ wafer covered with the insulating layer can also be applicable.

[0151] Further, it is also preferable to form the insulating layer on the surface of the above first base and thereafter bond it to the surface of the insulating layer of the second base, with the surface of the insulating layer of the first base being used as a bonding surface.

[0152] Since the insulating layer covering the surface of the second base acts as a barrier against penetration of a p-type impurity, the region immediately below the buried insulating layer becomes more resistant to decrease of the resistivity. Silicon oxide is preferably used as such an insulating layer, and the thickness of the insulating layer enough for the action as a barrier is not less than 100 nm and more preferably not less than 200 nm nor more than 10 μm.

[0153] The bonding surfaces of the first and second bases to be bonded can be bonded to each other more easily without formation of voids or the like at the bonding interface when the bonding surface of the first base is a surface comprised of a semiconductor of Si or the like and the other is a surface comprised of an insulator such as silicon oxide or the like.

[0154] In cases where surfaces of insulators are bonded to each other, it is more important to bond the surfaces after an element such as oxygen, nitrogen, silicon, or the like is introduced into at least one of the bonding surfaces by plasma ion implantation or the like.

(Embodiment 8)

[0155] Next described is Embodiment 8 resulting from partial modification of Embodiment 7 described above.

[0156] The surface of the p-type Si wafer as the first base 1 is anodized to make the surface porous. Then the semiconductor layer region 12 of non-porous single-crystal Si is formed on the porous surface by epitaxial growth.

[0157] Then the surface of the semiconductor layer region 12 is oxidized to form the insulating layer 2 as occasion may demand.

[0158] In this way, the first base is obtained as illus-

trated in Fig. 13A.

[0159] The second base 16 like the n-type FZ Si wafer of the high resistivity described in Embodiment 7 is prepared and the insulating layer 5 as a barrier is formed, fqr example, by thermal oxidation of at least the upper surface thereof or the like. Then the surface of at least one of the insulating layer 2 and the insulating layer 5 is subjected to a plasma process as occasion may demand. Then the second base, together with the first base, is placed in the bonding atmosphere having the low p-type impurity concentration (Np < Nn) and they are kept in close contact with each other. At this time a heat treatment is carried out at 900°C to 1200°C if necessary. The multi-layer structure as illustrated in Fig. 13B is obtained in this way.

[0160] After that, the non-porous part on the surface side of the first base 1 is removed by grinding, polishing, etching, or the like and the porous layer 11 is removed by selective wet etching with an etchant containing hydrogen fluoride and hydrogen peroxide, thereby obtaining the SOI substrate as illustrated in Fig. 13C.

[0161] Alternatively, a fluid or a wedge is driven against or into the side face of the multi-layer structure, or tension is applied in directions to separate the first base and the second base from each other, or the like, whereby the two members are separated from each other at the border of the porous layer with low mechanical strength, thereby obtaining the SOI substrate with the semiconductor layer region 12 being left on the second base.

[0162] Further, the substrate is subjected to a heat treatment in a reducing atmosphere of hydrogen 100 % or in a reducing atmosphere of hydrogen diluted with an inert gas for one or more hours, whereby the rough surface 19 of the semiconductor layer region is smoothed so that the surface roughness of the SOI substrate becomes sufficiently smooth to Rrms not more than 5 nm.

[0163] The SOI substrate as illustrated in Fig. 13D is obtained in this way.

[0164] Since in this SOI substrate the support substrate 16 below the buried insulating layer 2 has the sufficiently high resistivity of not less than 100 Ωcm and more preferably not less than 1000 Qcm, the transistor produced with this SOI substrate has less parasitic capacitance and can operate at a high speed.

(Embodiment 9)

[0165] Embodiment 9 is also an example resulting from partial modification of Embodiment 7.

[0166] As illustrated in Fig. 14A, the insulating layer 2 is formed on the surface of the first base 1 comprised of a semiconductor such as the Si wafer.

[0167] As illustrated in Fig. 14B, hydrogen ions or rare gas ions are implanted by ion implantation in the region about 100 nm to 2 μm below the lower surface of the insulating layer 2 of the first base 1 to form an ion-implanted layer 15 for creation of microbubbles. Then, it may be subjected to a heat treatment at 100°C to 400°C to evolve the microbubbles in the ion-implanted layer 15 if necessary.

[0168] As illustrated in Fig. 14C, the second base 16, which is comprised of a semiconductor such as the high-resistance n-type Si wafer or the like as described in Embodiment 7, is prepared, and the insulating layer 5 to become a barrier is formed on the surface thereof. The second base is then kept in close contact with the insulating layer 2 in the atmosphere 20N illustrated in Fig. 2. Then the substrate is subjected to a heat treatment at 500°C to 1200°C to aggregate the microbubbles evolved in the ion-implanted layer 15 or to newly evolve and aggregate the microparticles therein. Then the ion-implanted layer becomes fragile, and the first base 1 of the multi-layer structure is separated at the border of the ion-implanted layer 15 while the semiconductor layer region 12 is left.

[0169] Then the exposed surface of the semiconductor region 12 is smoothed by polishing or by a heat treatment in a reducing atmosphere containing hydrogen to obtain the SOI substrate with relatively good quality, though inferior to that of Embodiment 7, as illustrated in Fig. 14D.

[0170] The SOI substrate thus obtained is one with the support substrate having the resistivity profile as indicated by P31 of Fig. 12.

(Embodiment 10)

[0171] Fig. 15 is a schematic, sectional view of a semiconductor substrate according to the present invention.

[0172] This semiconductor substrate has a semiconductor layer region 41 of a single-crystal semiconductor through an insulating layer 42 on a support substrate 43 of a semiconductor, and the resistivity of semiconductor surface portion 44s immediately below the insulating layer 42 is not less than 100 Ωcm, more preferably not less than 500 Ωcm, and still more preferably not less than 1000 Ωcm.

[0173] Since the resistance of the semiconductor surface portion 44s is high as described above, the capacitance is low in the structure composed of the semiconductor layer region 41, the insulating layer 42, and the support substrate 43.

(Embodiment 11)

[0174] Fig. 16 is a schematic, sectional view of a semiconductor device according to the present invention.

[0175] This semiconductor device is produced by subjecting the semiconductor substrate illustrated in Fig. 15 to various processes and a transistor is fabricated in this semiconductor substrate.

[0176] In order to accomplish the LDD (Lightly Doped Drain) structure, source and drain regions 46, 47 of mutually different impurity concentrations are formed in the semiconductor layer region 41.

[0177] Numeral 45 designates an insulator for element isolation, 48 a gate electrode of polysilicon, silicide, metal, or the like, 49 a gate insulating film of silicon oxide or the like, 50 a channel region, 51 an insulating film, 52 source and drain electrodes of a metal such as aluminum, copper, or the like buried in contact holes formed in the insulating film 51, and 53 a barrier metal made of a high-melting-point metal (refractory metal), silicide, electrically conductive nitride, or the like.

[0178] An integrated circuit fabricated using the above-stated transistor according to the present invention demonstrates good high-frequency characteristics with little leak current and with a high cut-off frequency, because the region 44 near the semiconductor surface immediately below the buried insulating layer 42 has the high resistance.

[0179] Further, the transistor may also be any other transistor than the MOS transistor of the LDD structure; for example, a bipolar transistor or the like.

(Embodiment 12)

[0180] Embodiment 12 is an example in which there is a region with increasing resistivity toward the top in the figure in the vicinity 44 of the semiconductor surface in order to increase the resistance of the semiconductor surface portion 44s of the support substrate 43 illustrated in Fig. 15. Such a region with gradually increasing resistivity can be formed by forming a pn junction in the vicinity 44 of the semiconductor surface or by introducing a small amount of an impurity of the opposite conductivity type into the surface side of the semiconductor surface vicinity 44.

[0181] The present embodiment permits the resistivity of the semiconductor surface portion 44s of the support substrate 43 to be maintained readily in the range of not less than 100 Ωcm, more preferably in the range of not less than 500 Ωcm, and still more preferably in the range of not less than 1000 Ωcm.

(Example 1)

[0182] A CZ wafer of p-type (100) single-crystal Si having the diameter of 6 inches and the thickness of 600 μm was anodized in 50 % HF solution. The current density at this time was 10 mA/cm^2. A porous layer having the thickness of 20 μm was formed in the surface 10 minutes after. Then an Si epitaxial layer was grown in the thickness of 0.5 μm on this p-type porous Si layer by a low pressure CVD process. The deposition conditions were as follows.

Gas: SiH_2Cl_2 (0.6 liter/min), H_2 (100 liter/min)
Temperature: 850°C
Pressure: 50 Torr
Growth rate: 0.1 μm/min.

[0183] Next, the surface of this epitaxial layer was thermally oxidized by the thickness of 50 nm. A p-type FZ Si wafer having the resistivity of 5000 Ωcm was overlaid on the thermally oxidized film of the resultant CZ wafer in a clean air atmosphere having the boron concentration of 0.0003 ng/liter and the phosphorus concentration of 0.001 ng/liter by the use of the system as illustrated in Fig. 2 and the two wafers were bonded to each other firmly by heating them at 900°C for one and a half hours.

[0184] The concentrations of arsenic and antimony were negligibly lower than the boron concentration.

[0185] After that, the resultant substrate was ground by 580 μm from the back surface side of the CZ wafer, and then was subjected to reactive ion etching so as to expose the porous layer.

[0186] After that, the exposed porous layer underwent selective etching with a mixture solution of hydrofluoric acid and hydrogen peroxide. Only the single-crystal Si layer epitaxially grown was left without being etched 15 minutes after and the porous Si layer was completely removed selectively.

[0187] The etching rate of the non-porous Si single-crystal against the etchant was extremely low, approximately 40 Å even 15 minutes after, so that the etch selectivity of the etching rate of the porous Si layer was extremely large; therefore, etch amounts in the non-porous Si layer were almost practically negligible.

[0188] The SOI substrate formed in this way was put in a heat treatment furnace to be heat treated at 1150°C in a 100 % hydrogen atmosphere for four hours, thereby obtaining the SOI substrate smoothed to the surface roughness of Rrms = 2 nm or less.

[0189] The support substrate below the buried insulating layer in this substrate was analyzed by SIMS analysis and it was verified that phosphorus penetrated up to the area around 1 μm from the surface to increase the phosphorus concentration therein.

[0190] The resistivity profile of the substrate is one indicated by P14 of Fig. 17. It is thus seen that the layer region with increasing resistivity toward the surface (the region 0.5 μm to 1 μm deep) is formed near the surface of the support substrate.

(Example 2)

[0191] Before the bonding in Example 1, the surface of the p-type Si FZ wafer having the resistivity of 5000 Ωcm was thermally oxidized to form an insulating layer of silicon oxide in the thickness of 300 nm.

[0192] The bonding surface of the insulating layer was then exposed to a nitrogen plasma and thereafter the substrates, were bonded to each other in the low-boron-concentration atmosphere as in Example 1.

[0193] The SOI substrate was obtained in like manner as in Example 1 except for the above.

[0194] The resistivity profile of the surface of the support substrate of this SOI substrate was one indicated by P15 of Fig. 17. It is thus seen that the layer region

with gradually increasing resistivity toward the surface (the region 0 to 0.5 μm deep) is formed near the surface of the support substrate.

(Example 3)

[0195] A CZ wafer of p-type (100) single-crystal Si having the diameter of 6 inches and the thickness of 600 μm was anodized in 50 % HF solution. The current density at this time was 10 mA/cm^2. A porous layer having the thickness of 20 μm was formed in the surface 10 minutes after. Then an Si epitaxial layer was grown in the thickness of 0.5 μm on this p-type porous Si layer by the low pressure CVD process. The deposition conditions were as follows.

Gas: SiH_2Cl_2 (0.6 liter/min), H_2 (100 liter/min)
Temperature: 850°C
Pressure: 50 Torr
Growth rate: 0.1 μm/min.

[0196] Next, the surface of this epitaxial layer was thermally oxidized by the thickness of 50 nm. An n-type FZ Si wafer having the resistivity of 150 Ωcm was overlaid on the thermally oxidized film thus obtained, in a clean air atmosphere having the boron concentration of 0.004 ng/liter and the phosphorus concentration of 0.002 ng/liter by the use of the system as illustrated in Fig. 7 and the two wafers were bonded to each other firmly by heating them at 900°C for one and a half hours.

[0197] After that, grinding and reactive ion etching were carried out by 580 μm from the back surface side of the CZ wafer to expose the porous layer.

[0198] After that, the exposed porous layer underwent selective etching with the mixture solution of hydrofluoric acid and hydrogen peroxide. Only the single-crystal Si layer epitaxially grown was left without being etched 15 minutes after and the porous Si layer was completely removed selectively.

[0199] The SOI substrate formed in this way was put in the heat treatment furnace to be heat treated at 1150°C in a 100 % hydrogen atmosphere for four hours, thereby obtaining the SOI substrate smoothed to the surface roughness of Rrms = 2 nm or less.

[0200] The support substrate below the buried insulating layer in this substrate was analyzed by SIMS analysis and it was verified that boron penetrated up to the area around 1 μm from the surface to increase the boron concentration therein.

[0201] Further, the resistivity profile was similar to that indicated by P21 of Fig. 8. It was thus verified that a pn junction was formed in the layer region (the region 0 to 3 μm deep) near the surface of the support substrate.

(Example 4)

[0202] Before the bonding in Example 3, the surface of the n-type Si FZ wafer having the resistivity of 700 Ωcm was thermally oxidized to form an insulating layer of silicon oxide in the thickness of 300 nm.

[0203] The bonding surface of the insulating layer was then exposed to the nitrogen plasma and thereafter the substrates were bonded to each other in the high-boron-concentration atmosphere as in Example 3.

[0204] The SOI substrate was obtained in like manner as in Example 3 except for the above.

[0205] The resistivity profile of the surface of the support substrate of this SOI substrate was one indicated by P23 of Fig. 18. It was thus verified that a pn junction was formed in the layer region (the region 0 to 2 μm deep) near the surface of the support substrate.

(Example 5)

[0206] A CZ wafer of p-type (100) single-crystal Si having the diameter of 6 inches and the thickness of 600 μm was anodized in 50 % HF solution. The current density at this time was 10 mA/cm^2. A porous layer having the thickness of 20 μm was formed in the surface of the CZ wafer 10 minutes after. Then an Si epitaxial layer was grown in the thickness of 0.5 μm on this p-type porous Si layer by the low pressure CVD process. The deposition conditions were as follows.

Gas: SiH_2Cl_2 (0.6 liter/min), H_2 (100 liter/min)
Temperature: 850°C
Pressure: 50 Torr
Growth rate: 0.1 μm/min.

[0207] Besides it, an n-type FZ wafer having the resistivity of 6000 Ω·cm was prepared and the insulating layer becoming a barrier was formed in the thickness of 300 nm by thermal oxidation. The n-type FZ Si wafer having the resistivity of 6000 Ωcm and provided with the insulating layer was overlaid on the surface of the epitaxial layer in a clean air atmosphere having the boron concentration of 0.0003 ng/liter and the phosphorus concentration of 0.001 ng/liter by the use of the system as illustrated in Fig. 2 and the two wafers were bonded to each other firmly by heating them at 900°C for one and a half hours. The concentrations of arsenic and antimony were negligibly smaller than the boron concentration.

[0208] After that, grinding and reactive ion etching were carried out by 580 μm from the back surface side of the CZ wafer to expose the porous layer.

[0209] After that, the porous layer underwent selective etching with the mixture solution of hydrofluoric acid and hydrogen peroxide. Only the single-crystal Si layer was left without being etched 15 minutes after and the porous Si layer was completely removed selectively.

[0210] The SOI substrate formed in this way was put in the heat treatment furnace to be heat treated at 1150°C in the 100 % hydrogen atmosphere for four hours, thereby obtaining the SOI substrate smoothed to the surface roughness of Rrms = 2 nm or less.

[0211] The support substrate below the buried insulating layer in this substrate was analyzed by SIMS analysis and it was verified that phosphorus penetrated up to the area around 0.3 μm from the surface to increase the phosphorus concentration slightly therein.

[0212] Further, the resistivity profile of the substrate was similar to that indicated by P31 of Fig. 12.

(Example 6)

[0213] Example 6 is different from Example 5 in that prior to the bonding in Example 5, an insulating layer of silicon oxide 50 nm thick was formed by thermal oxidation of the surface of the epitaxial layer on the CZ wafer as the first base.

[0214] Then the bonding surface of the insulating layer was exposed to the nitrogen plasma and thereafter the bonding surfaces were bonded to each other in the low-boron-concentration atmosphere as in Example 5.

[0215] The SOI substrate was obtained in like manner as in Example 5 except for the above.

[0216] The resistivity profile of the surface of the support substrate in this SOI substrate was one as indicated by P31 of Fig. 12.

[0217] According to the present invention, when producing an SOI substrate, it is possible to restrain the resistivity of the vicinity of the surface of the support substrate from decreasing near the surface of the support substrate immediately below the insulating layer, thereby providing a semiconductor substrate that can be an SOI substrate suitable for production of high-frequency transistors.

Claims

1. A method of producing a semiconductor substrate comprising a step of bonding a first base comprising a semiconductor layer region to a second base and a step of removing the first base while leaving the semiconductor layer region on the second base,

   wherein according to the composition of the second base, a magnitude relation is established between the concentration of an n-type impurity and the concentration of a p-type impurity in an atmosphere for carrying out the bonding step.

2. The method of producing the semiconductor substrate according to Claim 1, wherein when at least a portion of the second base on the bonding surface side is an n-type semiconductor having a resistivity of not less than 100 Ωcm, the concentration of the n-type impurity is made lower than the concentration of the p-type impurity in the atmosphere in the bonding step, wherein when at least a portion of the second base on the bonding surface side is an n-type semiconductor having a resistivity of not less than 300 Ωcm and covered with an insulating layer, the concentration of the p-type impurity is made lower than the concentration of the n-type impurity in the atmosphere in the bonding step, and wherein when at least a portion of the second base on the bonding surface side is a p-type semiconductor having a resistivity of not less than 100 Ωcm, the concentration of the p-type impurity is made lower than the concentration of the n-type impurity in the atmosphere in the bonding step.

3. The method of producing the semiconductor substrate according to Claim 1 or 2, wherein the concentration of the p-type impurity is the concentration of boron and the concentration of the n-type impurity is the concentration of phosphorus.

4. the method of producing the semiconductor substrate according to Claim 1 or 2, wherein the concentration of the p-type impurity is the concentration of boron and is not more than 0.05 ng/liter, and wherein the concentration of the n-type impurity is the concentration of phosphorus and is not more than 0.1 ng/liter.

5. The method of producing the semiconductor substrate according to Claim 1 or 2, wherein the second base is an FZ silicon wafer.

6. The method of producing the semiconductor substrate according to Claim 1 or 2, wherein in or after the bonding step, a heat treatment is carried out at a temperature not less than 900°C.

7. The method of producing the semiconductor substrate according to Claim 1 or 2, wherein the resistivity of a semiconductor surface portion of the second base forming the semiconductor substrate is not less than 100 Ωcm.

8. The method of producing the semiconductor substrate according to Claim 1 or 2, wherein a region with increasing resistivity toward a surface of the second base is formed in the vicinity of the semiconductor surface of the second base forming the semiconductor substrate.

9. A semiconductor substrate having the SOI structure, which is produced by the method of producing the semiconductor substrate as set forth in Claim 1 or 2.

10. A semiconductor substrate having a semiconductor layer region comprising a single-crystal semiconductor through an insulating layer on a support substrate comprising a semiconductor,

    wherein the support substrate has such a composition that a semiconductor surface portion immediately below the insulating layer is a semicon-

ductor having a resistivity of not less than 100 Ωcm and/or such a composition that the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof.

11. The method of producing the semiconductor substrate according to Claim 1, wherein the bonding step is carried out in an atmosphere in which the concentration of the n-type impurity is lower than the concentration of the p-type impurity, and wherein the second base is a base comprising a portion comprising an n-type semiconductor having a resistivity of not less than 100 Ωcm on the bonding surface side.

12. The method of producing the semiconductor substrate according to Claim 11, wherein after an insulating layer is formed on a surface of the semiconductor layer region, the first base is bonded to the second base.

13. The method of producing the semiconductor substrate according to Claim 11, wherein the second base has an insulating layer on the bonding surface side.

14. The method of producing the semiconductor substrate according to Claim 11, wherein the concentration of the p-type impurity penetrating from the atmosphere into the second base is not less than 0.1 times nor more than 2 times the concentration of an n-type impurity in the second base.

15. The method of producing the semiconductor substrate according to Claim 11, wherein the second base is an FZ Si wafer.

16. The method of producing the semiconductor substrate according to Claim 11, wherein the atmosphere comprises clean air supplied through a boron-releasing filter.

17. The method of producing the semiconductor substrate according to Claim 11, wherein the n-type impurity is phosphorus.

18. The method of producing the semiconductor substrate according to Claim 11, wherein the p-type impurity is boron, and wherein the concentration of boron in the atmosphere is not more than 0.05 ng/liter.

19. The method of producing the semiconductor substrate according to Claim 11, wherein the n-type impurity is phosphorus, and wherein the concentration of phosphorus in the atmosphere is not more than 0.01 ng/liter.

20. The method of producing the semiconductor substrate according to Claim 11, wherein the first base comprises a porous layer and/or an ion-implanted layer.

21. The method of producing the semiconductor substrate according to Claim 11, wherein the semiconductor layer region comprises a single-crystal semiconductor epitaxially grown on a porous single-crystal layer.

22. The method of producing the semiconductor substrate according to Claim 11, wherein a heat treatment at 900°C or higher is carried out in the bonding step.

23. The method of producing the semiconductor substrate according to Claim 11, further comprising a step of carrying out a heat treatment to heat the semiconductor layer region left on the second base at 900°C or higher.

24. The semiconductor substrate according to Claim 10, wherein the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof near the insulating layer.

25. The semiconductor substrate according to Claim 24, wherein the support substrate has a p-type layer region to form a pn junction near the insulating layer.

26. The method of producing the semiconductor substrate according to Claim 1, wherein the bonding step is carried out in an atmosphere in which the concentration of the p-type impurity is lower than the concentration of the n-type impurity, and wherein the second base is a base comprising a portion comprising a p-type semiconductor having a resistivity of not less than 100 Ωcm on the bonding surface side.

27. The method of producing the semiconductor substrate according to Claim 26, wherein after an insulating layer is formed on a surface of the semiconductor layer region, the first base is bonded to the second base.

28. The method of producing the semiconductor substrate according to Claim 26, wherein the second base has an insulating layer on the bonding surface side.

29. The method of producing the semiconductor substrate according to Claim 26, wherein the concentration of the n-type impurity penetrating from the atmosphere into the second base is not less than 0.1 times nor more than 2 times the concentration

of a p-type impurity in the second base.

30. The method of producing the semiconductor substrate according to Claim 26, wherein the second base is an FZ Si wafer.

31. The method of producing the semiconductor substrate according to Claim 26, wherein the atmosphere comprises clean air supplied through a low-boron-releasing filter.

32. The method of producing the semiconductor substrate according to Claim 26, wherein the p-type impurity is boron.

33. The method of producing the semiconductor substrate according to Claim 32, wherein the concentration of the boron in the atmosphere is not more than 0.01 ng/liter.

34. The method of producing the semiconductor substrate according to Claim 26, wherein the n-type impurity is phosphorus, and wherein the concentration of phosphorus in the atmosphere is not more than 0.1 ng/liter.

35. The method of producing the semiconductor substrate according to Claim 26, wherein the first base comprises a porous layer and/or an ion-implanted layer.

36. The method of producing the semiconductor substrate according to Claim 26, wherein the semiconductor layer region comprises a single-crystal semiconductor epitaxially grown on a porous single-crystal layer.

37. The method of producing the semiconductor substrate according to Claim 26, wherein a heat treatment at 900°C or higher is carried out in the bonding step.

38. The method of producing the semiconductor substrate according to Claim 26, further comprising a step of carrying out a heat treatment to heat the semiconductor layer region left on the second base at 900°C or higher.

39. The semiconductor substrate according to Claim 10, wherein the support substrate has a region with increasing resistivity toward the insulating layer in the direction of thickness thereof near the insulating layer and a portion below the region comprises a p-type semiconductor or an n-type semiconductor.

40. The semiconductor substrate according to Claim 39, wherein the support substrate has a pn junction near the insulating layer.

41. The method of producing the semiconductor substrate according to Claim 1, wherein the bonding step is carried out in an atmosphere in which the concentration of the p-type impurity is lower than the concentration of the n-type impurity, and wherein the second base is a base comprising a portion comprising an n-type semiconductor having a resistivity of not less than 300 Ωcm and having an insulating layer formed on the bonding surface side.

42. The method of producing the semiconductor substrate according to Claim 41, wherein after an insulating layer is formed on a surface of the semiconductor layer region, the first base is bonded to the second base.

43. The method of producing the semiconductor substrate according to Claim 41, wherein the insulating layer is a layer of an oxide formed on the bonding surface side.

44. The method of producing the semiconductor substrate according to Claim 41, wherein the resistivity of the second base is not less than 500 Ω·cm.

45. The method of producing the semiconductor substrate according to Claim 41, wherein the second base is an FZ Si wafer.

46. The method of producing the semiconductor substrate according to Claim 41, wherein the atmosphere comprises clean air supplied through a low-boron-releasing filter.

47. The method of producing the semiconductor substrate according to Claim 41, wherein the p-type impurity is boron.

48. The method of producing the semiconductor substrate according to Claim 47, wherein the concentration of the boron in the atmosphere is not more than 0.01 ng/liter.

49. The method of producing the semiconductor substrate according to Claim 41, wherein the n-type impurity is phosphorus, and wherein the concentration of phosphorus in the atmosphere is not more than 0.1 ng/liter.

50. The method of producing the semiconductor substrate according to Claim 41, wherein the first base comprises a porous layer and/or an ion-implanted layer.

51. The method of producing the semiconductor substrate according to Claim 41, wherein the semiconductor layer region comprises a single-crystal semiconductor epitaxially grown on a porous single-

crystal layer.

52. The method of producing the semiconductor substrate according to Claim 41, wherein a heat treatment at 900°C or higher is carried out in the bonding step.

53. The method of producing the semiconductor substrate according to Claim 41, further comprising a step of carrying out a heat treatment to heat the semiconductor layer region left on the second base at 900°C or higher.

54. The semiconductor substrate according to Claim 10, wherein the support substrate has a region with decreasing resistivity toward the insulating layer in the direction of thickness thereof.

55. The semiconductor substrate according to Claim 54, wherein the support substrate is an FZ Si wafer.

56. A semiconductor device formed in the semiconductor substrate of Claim 10.

57. The semiconductor device according to Claim 56, which is a transistor.

FIG. 1A

FIG. 1B

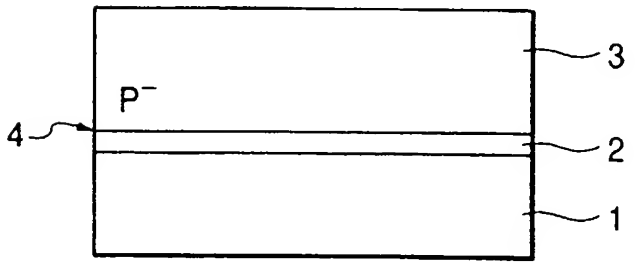


FIG. 1C

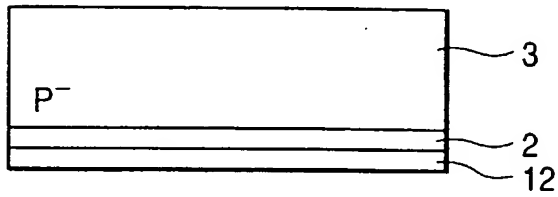


FIG. 2

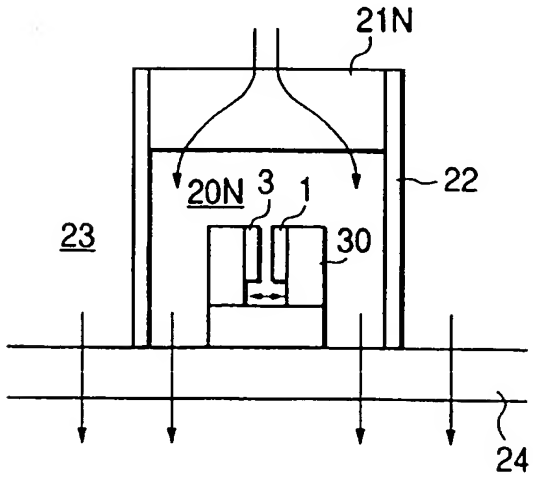


FIG. 3

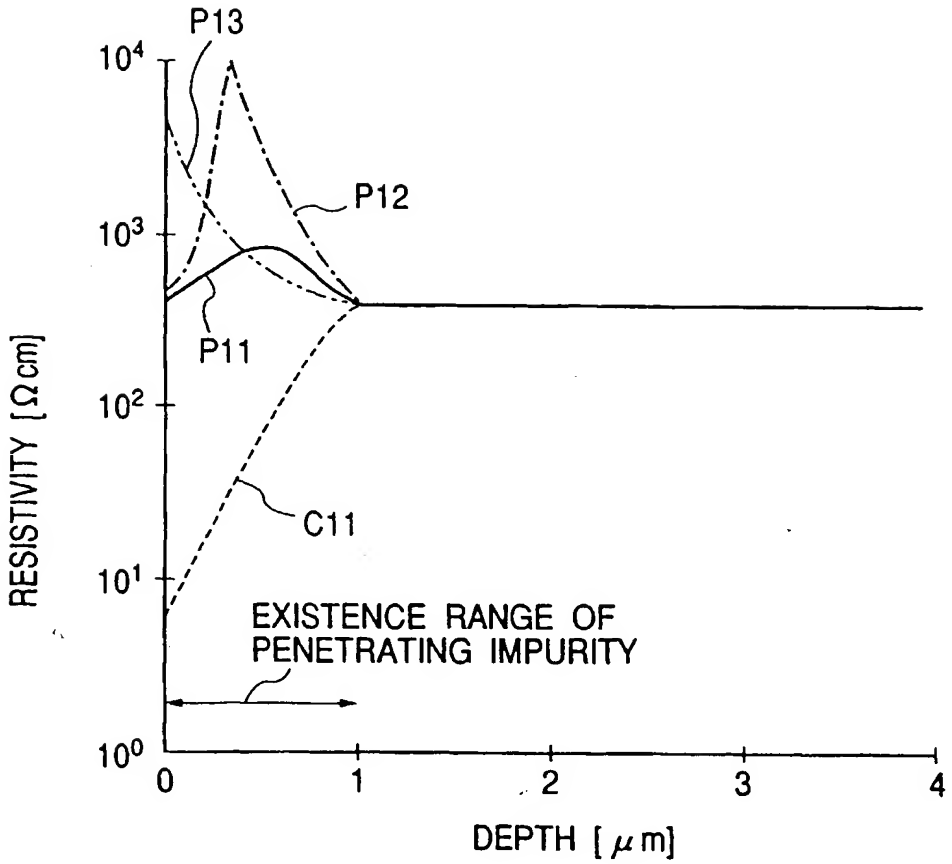


FIG. 4A

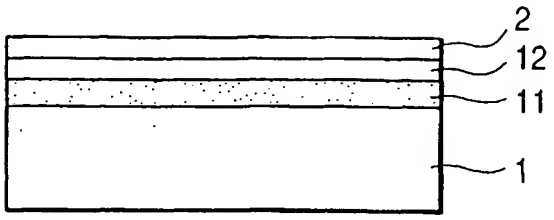


FIG. 4B

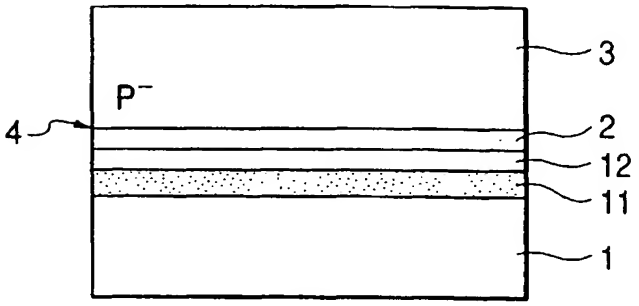


FIG. 4C

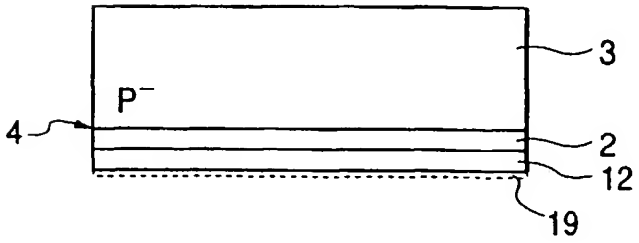


FIG. 4D

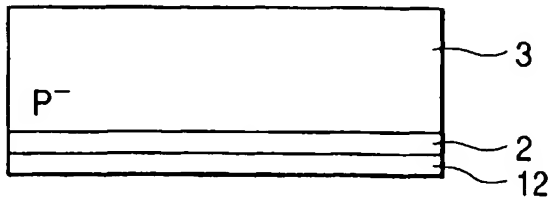


FIG. 5A

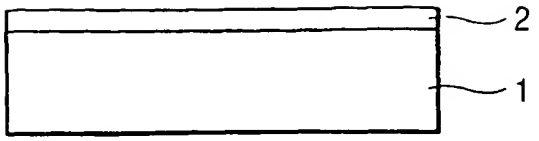


FIG. 5B

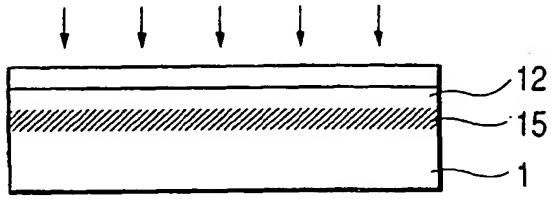


FIG. 5C

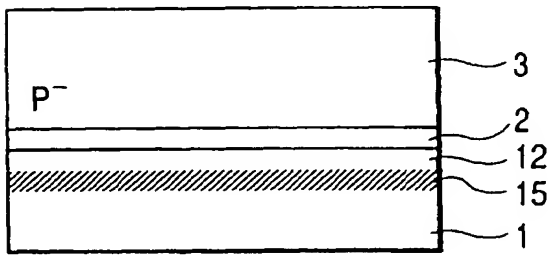


FIG. 5D

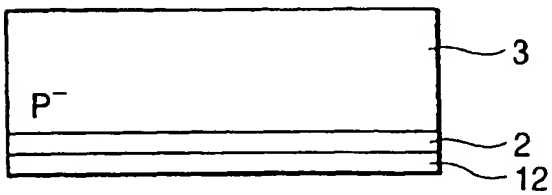


FIG. 6A

FIG. 6B

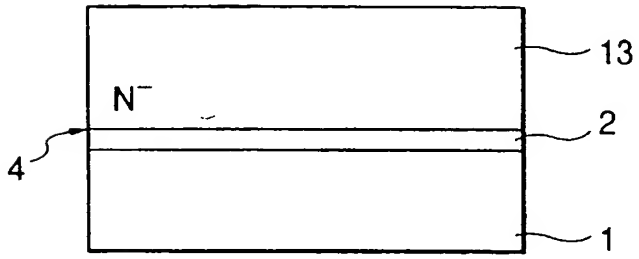


FIG. 6C

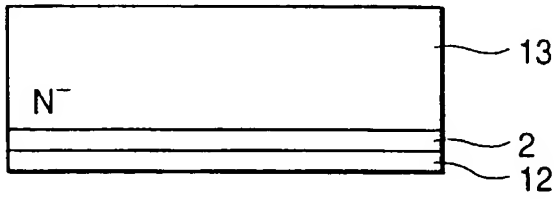


FIG. 7

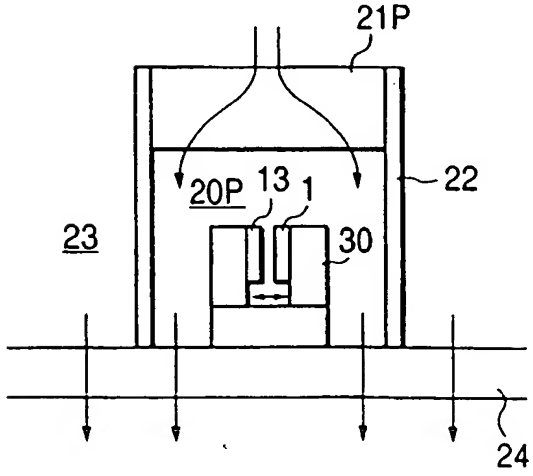


FIG. 8

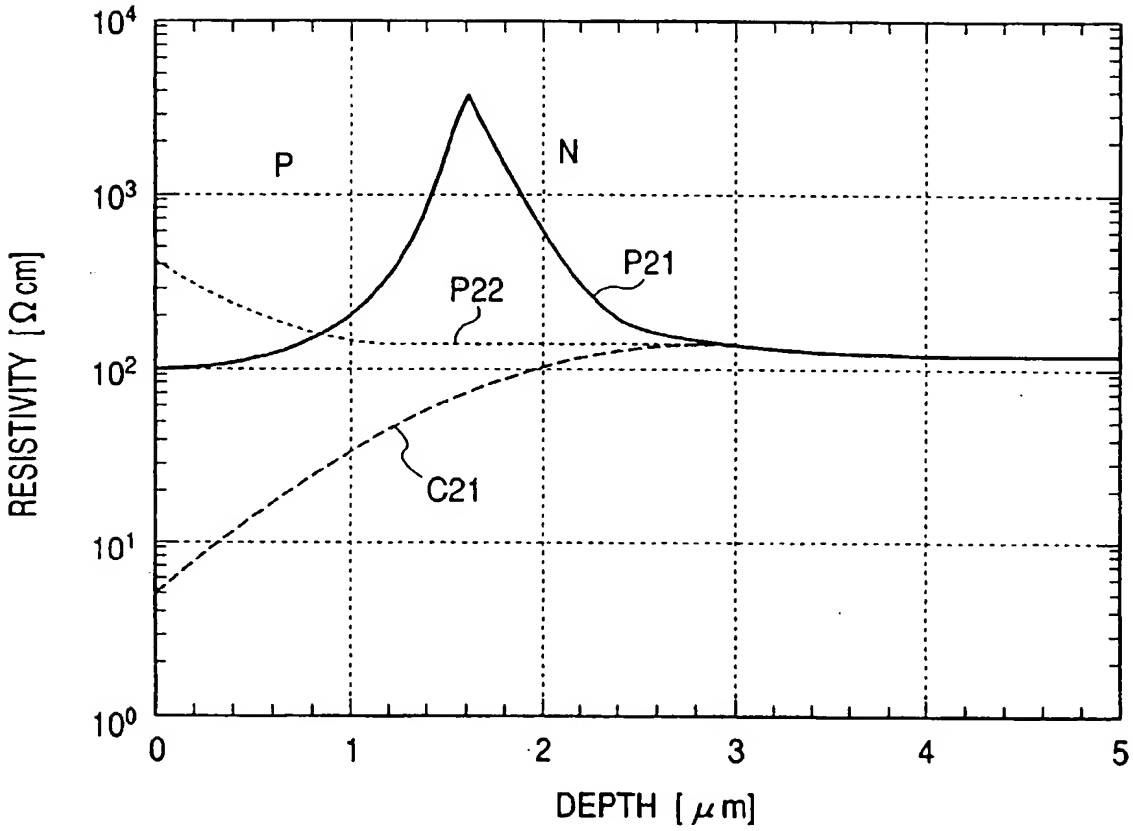


FIG. 9A

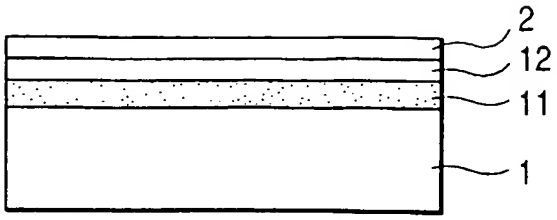


FIG. 9B

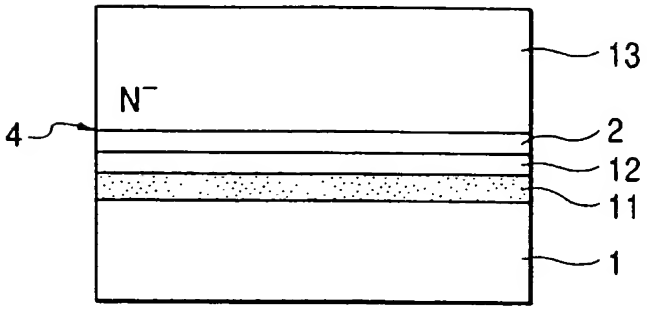


FIG. 9C

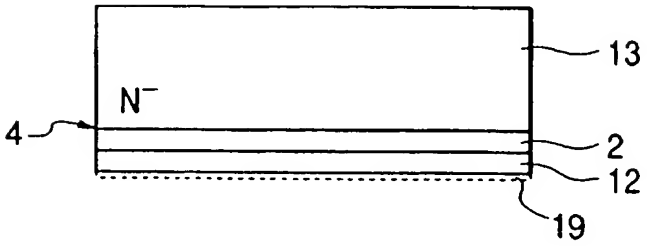


FIG. 9D

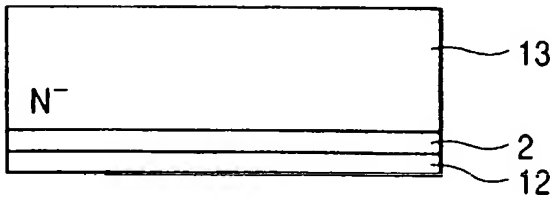


FIG. 10A

FIG. 10B

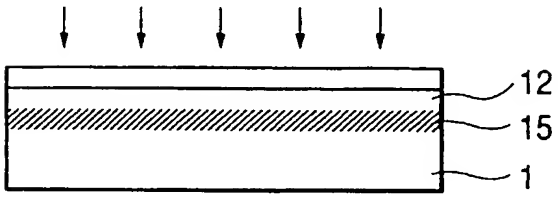


FIG. 10C

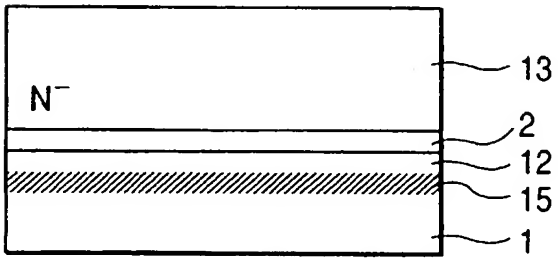


FIG. 10D

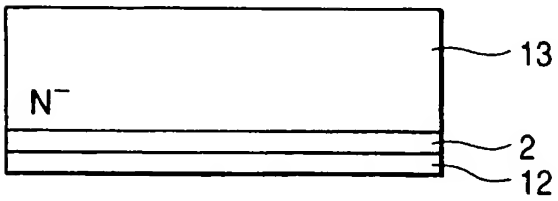


FIG. 11A

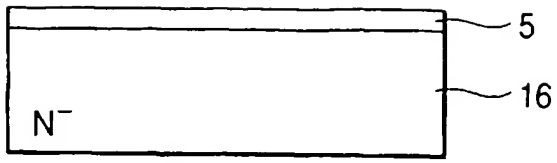


FIG. 11B

FIG. 11C

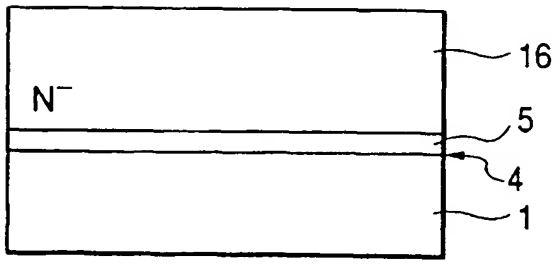


FIG. 11D

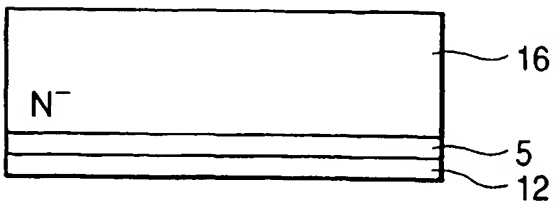


FIG. 12

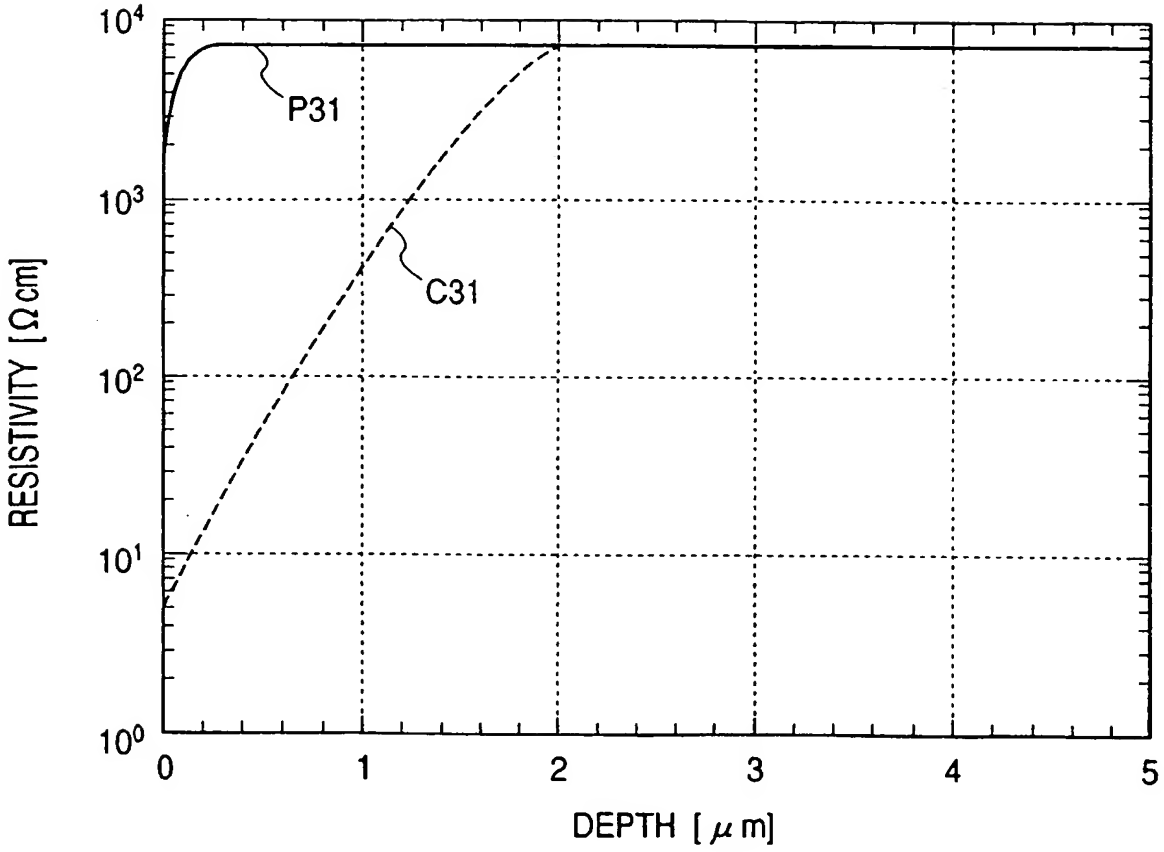


FIG. 13A

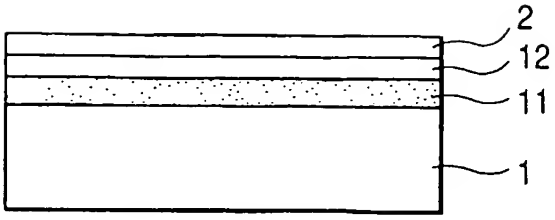


FIG. 13B

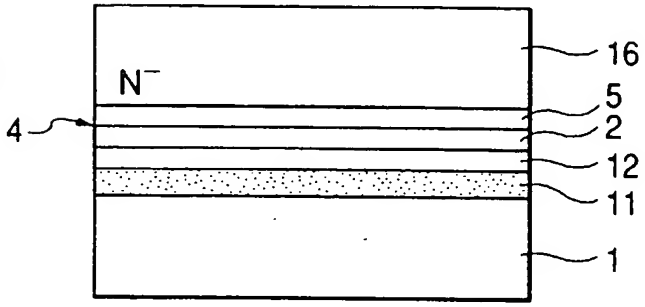


FIG. 13C

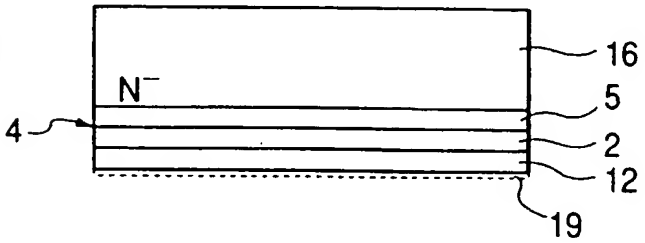


FIG. 13D

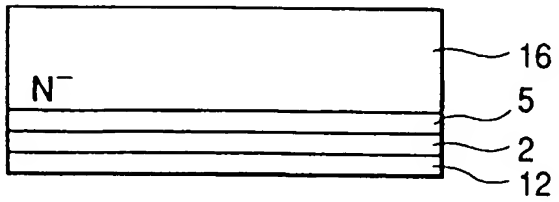


FIG. 14A

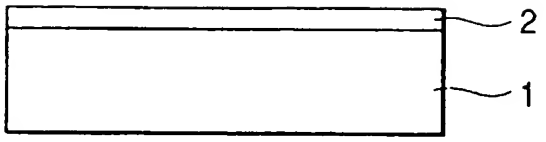


FIG. 14B

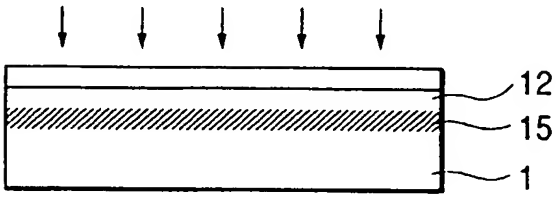


FIG. 14C

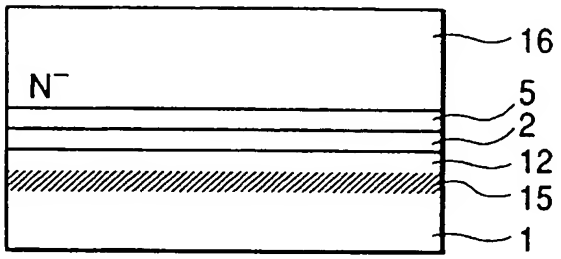


FIG. 14D

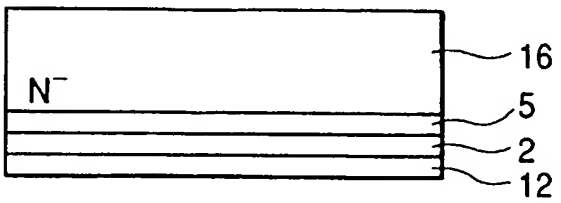


FIG. 15

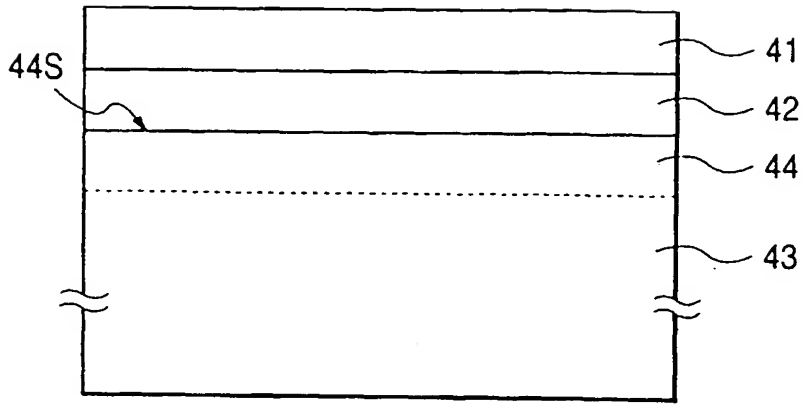

44S
41
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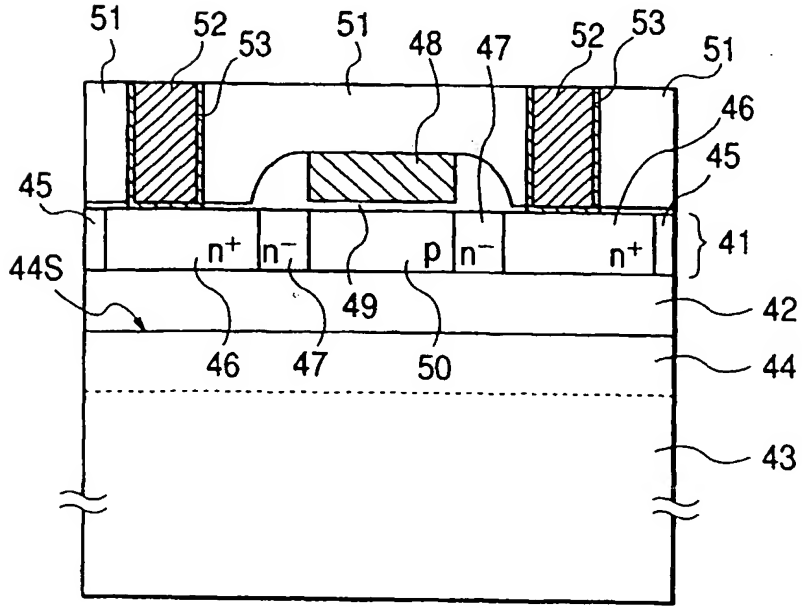
FIG. 16


51
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52
53
51
46
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n−
p
n−
n+
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44S
49
42
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43

FIG. 17

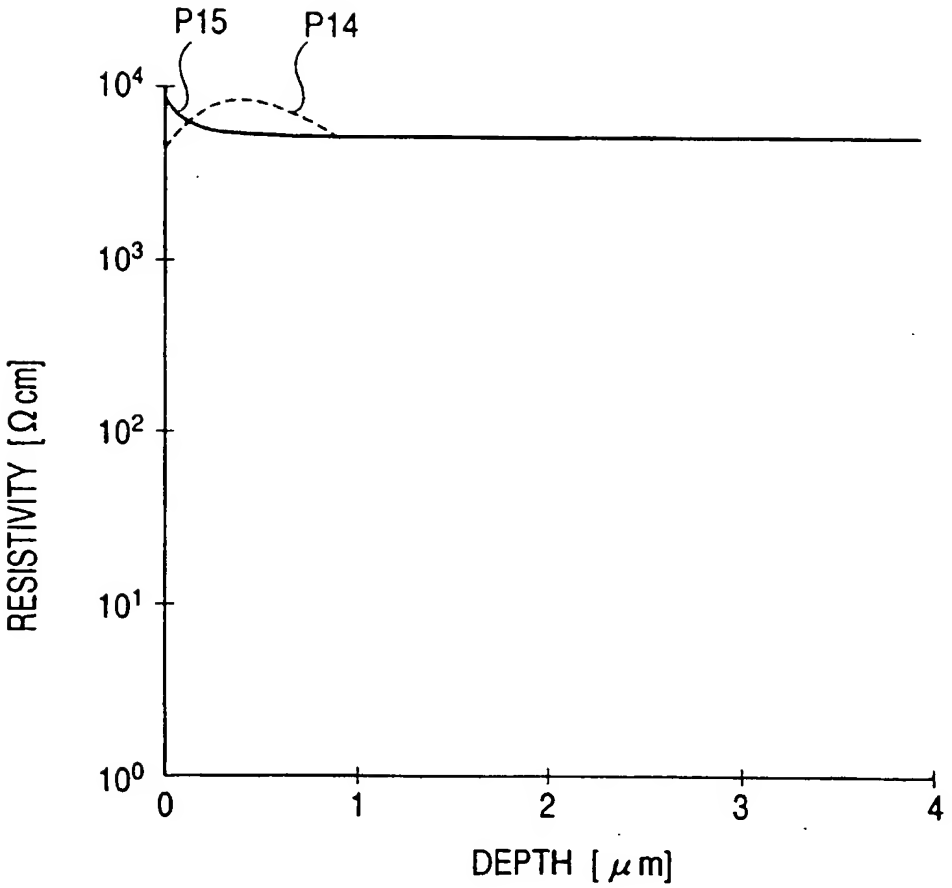


FIG. 18

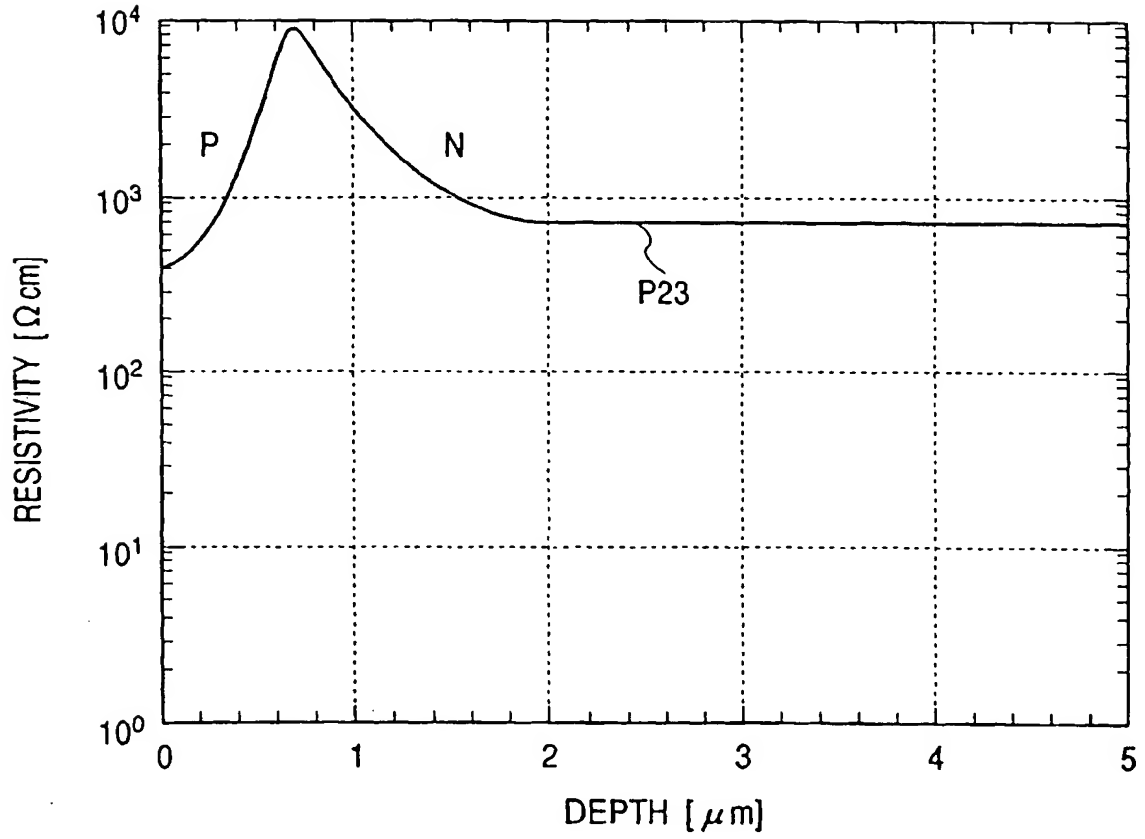


FIG. 19A

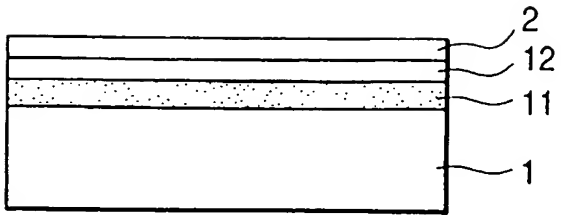


FIG. 19B

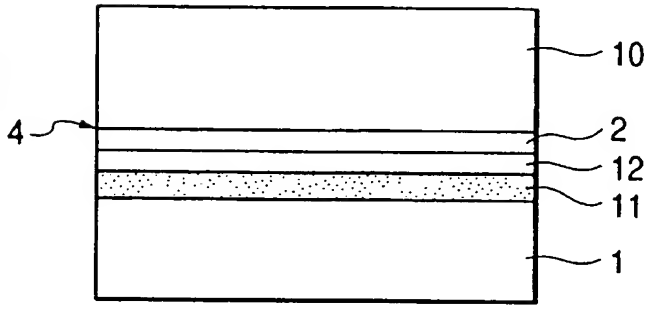


FIG. 19C

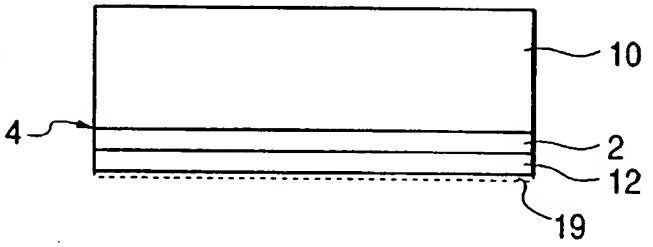
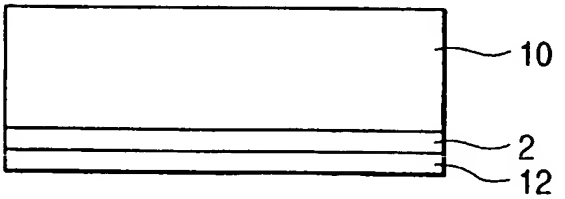


FIG. 19D



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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 5804

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 773 151 A (LOWTHER REX E ET AL) 30 June 1998 (1998-06-30) * abstract; claims; figures * * column 7, line 35 - line 45 *	10,24, 39,56,57	H01L21/20 H01L21/762
A	EP 0 767 486 A (CANON KK) 9 April 1997 (1997-04-09) * abstract; claims; figures *	1,11, 20-22, 26, 35-37, 41,50-52	
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 06, 31 July 1995 (1995-07-31) -& JP 07 058303 A (SHIN ETSU HANDOTAI CO LTD;OTHERS: 01), 3 March 1995 (1995-03-03) * abstract * -& US 5 804 494 A (KATAYAMA MASATAKE ET AL) 8 September 1998 (1998-09-08) * abstract; claims; figures *	1,9	
A	US 5 641 707 A (MOSLEHI MEHRDAD M) 24 June 1997 (1997-06-24) * abstract; claims; figures *	1,9	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24 November 1999	Wirner, C

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EPO FORM 1503 03.82 (P04C01)

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24-11-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5773151 A	30-06-1998	EP 0777911 A	11-06-1997
		WO 9702598 A	23-01-1997
EP 0767486 A	09-04-1997	JP 9162090 A	20-06-1997
		CA 2187269 A	07-04-1997
		CN 1159071 A	10-09-1997
		SG 63669 A	30-03-1999
		US 5854123 A	29-12-1998
JP 07058303 A	03-03-1995	JP 2723787 B	09-03-1998
		US 5804494 A	08-09-1998
US 5641707 A	24-06-1997	US 5866472 A	02-02-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82